Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (Canceled.)

21. (new) A method to manufacture a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

providing a processor core physically located upon a single integrated circuit;

providing one or more peripherals physically located upon said single integrated circuit; and

coupling a first internal bus physically located upon said single integrated circuit to said processor core and to said peripheral(s), said first internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said coupling of said first internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit; and

wherein adding said arbitrary number of pipeline stages to said first internal bus at floorplanning does not require a subsequent design or floorplanning iteration.

22. (new) The method of claim 21 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said method further comprises:

providing a memory subsystem physically located upon said single integrated circuit; and

coupling a second internal bus physically located upon said single integrated circuit to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said coupling of said second internal bus further comprises adding an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit; and

wherein adding said arbitrary number of pipeline stages to said second internal bus at floorplanning does not require a subsequent design or floorplanning iteration.

23. (new) The method of claim 21 or claim 22, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

24. (new) The method of claim 21 or claim 22, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

25. (new) The method of claim 22, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

26. (new) A method to use a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

initiating and receiving signals using a processor core physically located upon a single integrated circuit;

initiating and receiving signals using one or more peripherals physically located upon said single integrated circuit; and

carrying signals from signal initiators to signal targets using a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s), said first internal bus has a latency tolerant signal protocol;

wherein said first internal bus further comprises an arbitrary number of pipeline stages, wherein one or more of said arbitrary number of pipeline stages has been added between any signal initiator and any signal target when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration.

27. (new) The method of claim 26 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said method further comprises:

initiating and receiving signals using a memory subsystem physically located upon said single integrated circuit; and

carrying signals from signal initiators to signal targets using a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus has a latency tolerant signal protocol;

wherein said second internal bus further comprises an arbitrary number of pipeline stages, wherein one or more of said arbitrary number of pipeline stages has been added between any signal initiator and any signal target when floorplanning said single integrated circuit; and

wherein adding said one or more of said arbitrary number of pipeline stages to

said second internal bus at floorplanning does not require a subsequent design or floorplanning iteration.

28. (new) The method of claim 26 or claim 27, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

29. (new) The method of claim 26 or claim 27, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

30. (new) The method of claim 27, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

31. (new) A System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

a processor core physically located upon a single integrated circuit;

one or more peripherals physically located upon said single integrated circuit; and

a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s), said first internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated

circuit without requiring a subsequent design or floorplanning iteration.

32. (new) The apparatus of claim 31 wherein said one or more peripherals further comprises one or more DMA-type peripherals, further comprising:

a memory subsystem physically located upon said single integrated circuit; and

a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said second internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration.

33. (new) The apparatus of claim 31 or claim 32, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

34. (new) The apparatus of claim 31 or claim 32, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

35. (new) The apparatus of claim 32, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

36. (new) A system that includes a System-on-Chip (SOC) having a latency-tolerant architecture, comprising:

a processor core physically located upon a single integrated circuit;

one or more peripherals physically located upon said single integrated circuit; and

a first internal bus physically located upon said single integrated circuit coupled to said processor core and to said peripheral(s), said first internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said first internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target, one or more of said arbitrary number of pipeline stages having been added when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning iteration.

37. (new) The system of claim 36 wherein said one or more peripherals further comprises one or more DMA-type peripherals, further comprising:

a memory subsystem physically located upon said single integrated circuit; and

a second internal bus physically located upon said single integrated circuit coupled to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus has a latency tolerant signal protocol and carries signals from signal initiators to signal targets;

wherein said second internal bus further comprises an arbitrary number of pipeline stages between any signal initiator and any signal target when floorplanning said single integrated circuit without requiring a subsequent design or floorplanning

iteration.

38. (new) The system of claim 36 or claim 37, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

39. (new) The system of claim 36 or claim 37, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

40. (new) The system of claim 36, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.